Electronic Information Disclosure Statement

INTEGRATED CIRCUITS WITH PARALLEL SELF-TESTING

#2

Application:
Confirmation:
Applicant(s): Raj Kumar Jain
Docket Number: 2000P19153US
Group Art 2818
Examiner: THONG LE
search string: (4193125 or 4639892 or 5293386 or 5394354 or 5414653 or 5535164 or 5541872 or 5764588 or 5856940 or 5963468 or 6067265 or 6147895 or 6421797).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Citation No.	Patent Number	Date	Bar Code	Patentee	Class	Subclass
TL	P01	4193125	1980-03-11		Moriya	365	104
TL	P02	4639892	1987-01-27		Mizugaki et al	365	182
TL	P03	5293386	1994-03-08		Muhmenthaler et al	371	21.1
TL	P04	5394354	1995-02-28		Watabe et al	365	51
TL	P05	5414653	1995-05-09		Onishi et al	365	145
TL	P06	5535164	1996-07-09		Adams et al	365	201
TL	P07	5541872	1996-07-30		Lowrey et al	365	145
TL	P08	5764588	1998-06-09		Nogami et al	365	230.05

TL	P09	5856940	1999-01-05	[redacted]	Rao	365	149
TL	P10	5963468	1999-10-05	[redacted]	Rao	365	149
TL	P11	6067265	2000-05-23	[redacted]	Mukunoki et al	365	210
TL	P12	6147895	2000-11-14	[redacted]	Kamp	365	145
TL	P13	6421797	2002-07-16	[redacted]	Kim	714	718

Remarks

(Remarks are not for responding to an office action.)

Takashima D. & Kunishima I, "High-Density Chain Ferroelectric Random Access Memory (Chain FRAM)," May 1998, IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, Pg. 787-792

Signature

Examiner Name	Date
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